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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/532,398	03/22/2000	Paul A. Boerger	10991888-1	8092

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/532,398	BOERGER ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-29* is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. *This office action is in response to applicant's amendment filed 2 November 2004. Claims 1-29 are currently pending in this application. Claims 16-29 were previously allowed over the prior art of record. Claims 1-15 remain rejected.*

Response to Arguments

2. *Applicant's arguments filed 2 November 2004 have been fully considered.*

Regarding applicant's response to 112(1) rejection: The examiner first notes that applicant's arguments relating the definition of the term "simulation" are puzzling since applicant's invention is clearly directed toward computer simulation. The "preferred embodiment" on Page 3, line 6 of applicant's specification recites the following:

> *FIG. 1 is a block diagram of a capture exposure system 100.* ***Central processing unit (CPU) 110*** *sends illumination control signal 116 to LED driver 112 and LED model 102. LED driver 112 is coupled to LED array 114. LED array 114 provides illumination for capturing an image. LED model provides analog voltage 118 that tracks the light output of the LED'S in LED array 114. Analog voltage 118 is input to analog-to-digital converter (A/D converter) 104. The* ***output of A/D converter 104 is read by CPU 110****. This capture exposure system also has an ambient temperature sensor 106. The output of ambient temperature sensor 106 is read by A/D converter 104 and passed to CPU 110.* ***CPU 110 uses these two values to calculate*** *an exposure time for an image capture.*

In a nutshell, applicant's invention as disclosed in the specification, requires that the computer (CPU 110) and analog to digital converters (A/D converter 104) shown in Figure 1, be "in the loop", with the LED model, otherwise, the invention cannot operate. This clearly meets "narrow" Microsoft Dictionary definition of the term "simulation" cited in the examiner's previous office action as it would be known to any skilled artisan. Applicant's now appear to argue that the claimed "simulation" is simply carried out by the resistor and capacitor (R/C) circuit shown in figure 2 and does not involve a

computer at all. However, this is impossible since the circuit of figure 2 is passive, and hence does nothing unless excited by the illumination control signal from the CPU (computer). That is, the simulation requires the CPU as part of the model and is clearly a computer simulation. Therefore, in the interest of compact prosecution, and to simplify the issues in the case, the examiner assumes that applicants intend the meaning to the term "simulation circuit" to be inclusive of the CPU, A/D converter, and simple R/C model as noted above, and therefore withdraws the 112(1) rejection. That is, applicants are claiming a computer based "closed loop" simulation of the illumination source as part of an image capture exposure system that includes a CPU, A/D converter, and simple LED (R/C) model.

Regarding applicant's response to 102/103 rejection: Applicant's argue that Muratama does not disclose, or mention, anything similar to a model or simulation circuit and that the claimed circuits of the present invention are not computer algorithms, but instead are merely circuits. In response, the examiner first notes that both Muratama, and the claimed invention are drawn to the solving the same problem. Namely, that of maintaining a constant exposure in an image capture system, by compensating for the fact that the light output of an LED changes as a function of junction temperature. (i.e. illumination compensation, See: Applicant's specification: page 1, line 17 to page 2, line 9, Murata: CL4-L53-67) As noted above in arguments relating to the 112(1) rejection, applicant's arguments relating to exactly what comprises the claimed "simulation circuit" are somewhat ambiguous since applicants now appear to argue the "simulation circuit" consists only of the simple (and very well-known) R/C

circuit disclosed in figure 2. Since this circuit is passive, and is inoperative unless excited by the illumination control signal from the CPU (computer), the examiner has interpreted the claimed "simulation circuit" to be inclusive of the CPU, A/D converter, and simple LED (R/C) model (i.e. the exposure control circuit) as previously cited above. Against this backdrop, Muratama clearly teaches an exposure (illumination) control circuit that includes a CPU, digital conversion circuitry, an LED model (Fig. 4) and an exposure control model (Fig. 5, i.e. steps ST11-16). Since the broad language of the claim does not specify specifically what comprises the "simulation circuit", and since applicants now appear to argue that the simulation circuit is simply an inoperative R/C circuit, the examiner interprets the exposure control circuit disclosed by Muratama to be functionally equivalent to the claimed limitations of claims 1-5, 8-12, and 15.

MPEP 2106 further recites the following supporting rational:

"Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. > E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily).< In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.").
Where means plus function language is used to define the characteristics of a machine or manufacture invention, claim limitations must be interpreted to read on only the structures or materials disclosed in the specification and "equivalents thereof." (Two en banc decisions of the Federal Circuit have made clear that the Office is to interpret means plus function language according to 35 U.S.C. 112, sixth paragraph. In the first, In re Donaldson, 16 F.3d 1189, 1193, 29 USPQ2d 1845, 1848 (Fed. Cir. 1994), the court held:

Since the language of the claims and applicants arguments both offer multiple interpretations of the claimed limitations, the examiner maintains the rejection of claims 1-5, 8-12, and 15 under 35 USC 102/103 as cited below. Claims 6, 7, 13, 14 also remain rejected under 35 USC 103(a) as noted below.

Claim Interpretation

3. Since as cited above, applicant's specification is deficient in supporting the claimed limitations relating to a simulation circuit and simulating an illumination source using a circuit, the examiner has interpreted these limitations be a hardware circuit modeling an illumination source, and hence, functionally equivalent to the illumination modeling as disclosed in the prior art. (See 112(1) above, and 102(b)/103(a) below)

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In the alternative,

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-5, 8-12, and 15 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent 6,130,700 issued to Murayama et al or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. Patent 6,130,700 issued to Murayama et al in view of "Solid State Devices and Applications", F. Driscoll, pp. 370-380, Prentice-Hall Inc. 1975.

Amended independent claim 1 is drawn to an ***image capture device*** *including:*
Illumination source connected to power
Illumination source simulation circuit (model) with input/output
Exposure adjustment compensating for illumination changes indicated by circuit
Amended independent claim 8 includes additional limitations relating to:
Applying a potential to the illumination source
Monitoring the output
Adjusting the exposure

Regarding independent claims 1, and 8: Murayama discloses an image capture device incorporating an illumination source (model) consisting of light emitting elements including correction for environmental conditions (exposure time, ambient temperature, etc.) and modeling dynamically changing current and voltage to the illumination source (LED's) (Abstract, Background, Summary of Invention, CL4-L25-CL5-L20, CL5-L49-CL9-L20, CL9-L32, CL14-L51, Figs. 2-11)

Specifically, Murayama discloses an ***image capture device*** *with the elements of the claimed limitations of the present invention as follows:*

- Illumination source connected to power: (CL2-L13-15, Summary, Figs. 1-4)

- Illumination source simulation (model) circuit with input/output: The examiner asserts that the illumination source circuit model disclosed by Murayama is functionally equivalent to this claimed limitation (Summary, CL9-L20-CL14-L49, Figs. 2-6)

- Exposure adjustment compensating for illumination changes indicated by circuit: (Abstract, Background, Summary, CL5-L49-CL6-L24, Figs. 4-6)

- Applying a potential to the illumination source: (CL9-L37-60, Figs. 2-6)

- Monitoring the output: CPU 25 in Figure 4 monitors output of light (illumination) source. (CL9-L32, CL14-L51, Figs. 2-11)

- Adjusting the exposure responsively: (Abstract, Background, Summary, CL5-L49-CL6-L24, Figs. 4-6)

Per dependent claims 2-5, 9-12 and 15: Murayama discloses features relating to ambient temperature sensing, switching (on/off) times, and exposure adjustment as cited above.

In the alternative, the limitations relating to simulating the characteristics of a Light Emitting Diode (LED) recited in claims 1-5, 8-12, and 15 are rejected under 35 USC 103(a) as obvious in view of "Solid State Devices and Applications", F. Driscoll, pp. 370-380, Prentice-Hall Inc. 1975.

Per claims 1-5, 8-12, and 15: Murayama discloses an ***image capture device*** *with the elements of the claimed limitations of the present invention as previously cited*

above. Driscoll discloses the specific physical process for mathematically describing LED behavior. (pages 370-380, Figs. 10-12 to 10-16) As previously noted by the examiner, the term "simulation" is defined in the art as "The imitation of a physical process or object by a program that causes a computer to respond mathematically to data and changing conditions as though it were the process or object itself" (Microsoft Press Computer Dictionary, Third Edition, 1997) Hence, a skilled artisan would have known to use the physical process teachings of Driscoll to realize a simulation of an LED behavior. Accordingly, It would have been obvious to one skilled in the art at the time the claimed invention was made, to modify the teachings of Murayama relating to and image capture device, with the teachings of Driscoll relating to the specific physical process for mathematically describing LED, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of image capture devices available in the market place and large amounts of money being spent in product development and improvement. (see Murayama Background, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Murayama with the teachings of Driscoll in order to reduce development time and cost.

The examiner also notes that, as is known in the art and disclosed by Driscoll, in an LED the light output is a function of forward current. Luminous intensity (brightness), wavelength (hue or color), and forward voltage are the three main parameters of an LED that are affected by temperature. When compared to room (ambient) temperature,

higher temperatures cause the luminous intensity to slightly decrease (dimmer), the wavelength slightly lengthens (shifts towards red spectrum), and the forward voltage slightly decreases. Colder temperatures cause the luminous intensity to increase (brighter), the wavelength slightly shortens (shifts towards blue spectrum), and the forward voltage slightly increases. These parameters are generally described in the LED manufacturers data sheet and are compensated for in the prior art (Murayama). Accordingly, it would have been obvious to a skilled artisan (and necessary for the circuit to operate properly), to adjust the exposure based on the sensed ambient temperature, and hence, would have been incorporated as an inherent part of the cited prior art, and the claimed invention's illumination model. Further, because LED's are current devices they behave unpredictably when the applied voltage is varied, therefore the technique of pulse width modulation (i.e. switching on and off) is generally used to maintain a constant current and light output. Accordingly, a skilled artisan would have known to incorporate features relating to on times and off times into the model of the illumination source.

Dependent claims 6, 7, 13, 14 are rejected under 35 USC 103(a) in further view of "Microelectronic Circuits", A. S. Sedra, Holt, Rinehart, and Winston Inc. pp. 193-194, 1987.

Per dependent claims 6, 7, 13, 14: Sedra discloses a simple circuit for modeling a diode's resistance as a resistor with a capacitor representing the diode's diffusion capacitance. (See: Fig. 4.31) Hence, a skilled artisan would have known (and been

motivated as noted above) to us a simple resistor-capacitor circuit model to approximate the light output of the LED.

Allowable Subject Matter

5. The following is a statement of reasons for the indication of allowable subject matter:

Claims 16 and 23 use "mean for" language and are given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. § 112 paragraph 6. The "means for" language and the limitations related thereto of claims 16 and 23 are interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. Specifically, the modeling means, sensor means, and exposure adjustment means are interpreted as the specific sequence of steps disclosed in applicant's specification on page 3, line 16 to page 9, line 17. Claims 17-22 and 24-29 are allowable as depending from claims 16 and 23 respectively.

Conclusion

6. ***THIS ACTION IS MADE FINAL.*** *Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,087,846 issued to Alvord et al teaches LED light output testing and measuring.

PCT WO 01/27910 A1 issued to Silvestre teaches illumination measuring.

U.S. Patent 6,127,783 issued to Pashley et al teaches LED illumination detection.

"The Investigation of CCD Cameras and Image Processing Techniques for the Large Adaptive Reflector CCD Camera Based surface Measurement System", B. Carlson, Image Processing for LAR surface Measurement, April 12, 1999 - teaches image capture and LED compensation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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